

TC74LCX74F, TC74LCX74FN, TC74LCX74FT

LOW VOLTAGE DUAL D-TYPE FLIP FLOP WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX74 is a high performance CMOS D-TYPE FLIP FLOP. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for inputs.

The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.

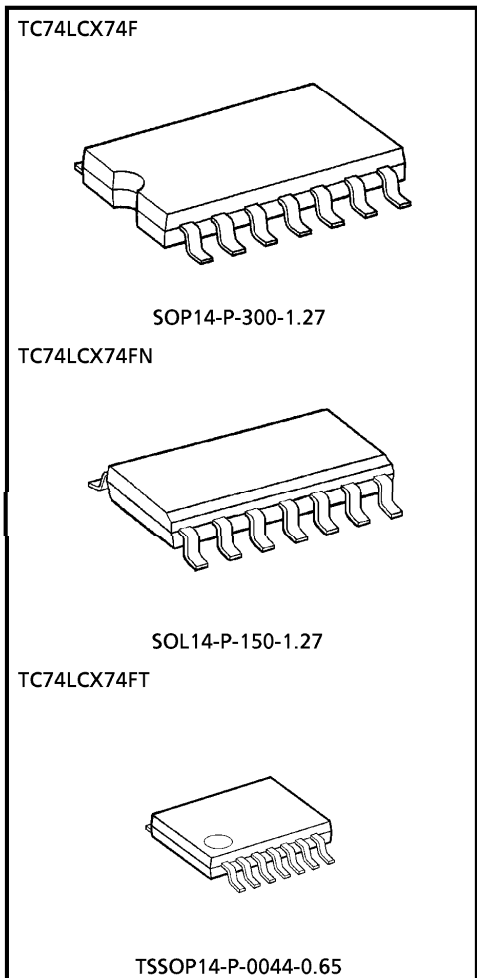
\overline{CLR} and \overline{PR} are independent of the CK and are accomplished by setting the appropriate input low.

All inputs are equipped with protection circuits against static discharge.

FEATURES

- Low voltage operation : $V_{CC} = 2.0 \sim 3.6V$
- High speed operation : $t_{pd} = 7.0ns$ (Max.)
($V_{CC} = 3.0 \sim 3.6V$)
- Output current : $|I_{OH}| / I_{OL} = 24mA$ (Min.)
($V_{CC} = 3.0V$)
- Latch-up performance : $\pm 500mA$
- Available in JEDEC SOP, EIAJ SOP and TSSOP
- Power down protection is provided on all inputs and outputs.
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 74 type.

(Note) The JEDEC SOP (FN) is not available in Japan.



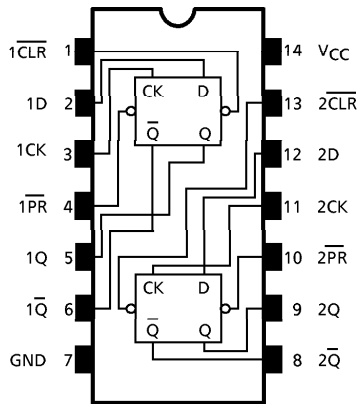
Weight

SOP14-P-300-1.27	: 0.18g (Typ.)
SOL14-P-150-1.27	: 0.12g (Typ.)
TSSOP14-P-0044-0.65	: 0.06g (Typ.)

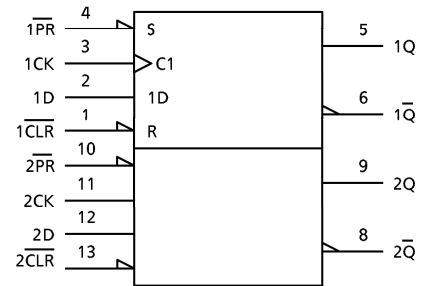
961001EBA2

● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
CLR	PR	D	CK	Q	Q̄	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	⏚	L	H	—
H	H	H	⏚	H	L	—
H	H	X	⏚	Q _n	Q̄ _n	NO CHANGE

X : Don't care

MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V _{CC}	-0.5~7.0	V
DC Input Voltage	V _{IN}	-0.5~7.0	V
DC Output Voltage	V _{OUT}	-0.5~7.0 (Note 1)	V
		-0.5~V _{CC} +0.5 (Note 2)	
Input Diode Current	I _{IK}	-50	mA
Output Diode Current	I _{OK}	±50 (Note 3)	mA
DC Output Current	I _{OUT}	±50	mA
Power Dissipation	P _D	180	mW
DC V _{CC} /Ground Current	I _{CC} /I _{GND}	±100	mA
Storage Temperature	T _{stg}	-65~150	°C

(Note 1) V_{CC} = 0V

(Note 2) High or Low State. I_{OUT} absolute maximum rating must be observed.

(Note 3) V_{OUT} < GND, V_{OUT} > V_{CC}

961001EBA2'

- The products described in this document are subject to foreign exchange and foreign trade control laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC}	2.0~3.6	V
		1.5~3.6 (Note 4)	
Input Voltage	V _{IN}	0~5.5	V
Output Voltage	V _{OUT}	0~5.5 (Note 5)	V
		0~V _{CC} (Note 6)	
Output Current	I _{OH} /I _{OL}	±24 (Note 7)	mA
		±12 (Note 8)	
Operating Temperature	T _{opr}	-40~85	°C
Input Rise And Fall Time	dt/dv	0~10 (Note 9)	ns/V

- (Note 4) Data Retention Only
- (Note 5) V_{CC} = 0V
- (Note 6) High or Low State
- (Note 7) V_{CC} = 3.0~3.6V
- (Note 8) V_{CC} = 2.7~3.0V
- (Note 9) V_{IN} = 0.8~2.0V, V_{CC} = 3.0V

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = -40~85°C)

PARAMETER		SYMBOL	TEST CONDITION	V _{CC} (V)	MIN.	MAX.	UNIT	
Input Voltage	"H" Level	V _{IH}		2.7~3.6	2.0	—	V	
	"L" Level	V _{IL}		2.7~3.6	—	0.8		
Output Voltage	"H" Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100μA	2.7~3.6	V _{CC} - 0.2	—	V
				I _{OH} = -12mA	2.7	2.2	—	
				I _{OH} = -18mA	3.0	2.4	—	
				I _{OH} = -24mA	3.0	2.2	—	
	"L" Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100μA	2.7~3.6	—	0.2	
				I _{OL} = 12mA	2.7	—	0.4	
				I _{OL} = 16mA	3.0	—	0.4	
			I _{OL} = 24mA	3.0	—	0.55		
Input Leakage Current	I _{IN}	V _{IN} = 0~5.5V		2.7~3.6	—	±5.0	μA	
Power Off Leakage Current	I _{OFF}	V _{IN} / V _{OUT} = 5.5V		0	—	10.0	μA	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND		2.7~3.6	—	10.0	μA	
		V _{IN} / V _{OUT} = 3.6~5.5V		2.7~3.6	—	±10.0		
Quiescent In I _{CC} Per Input	ΔI _{CC}	V _{IH} = V _{CC} - 0.6V		2.7~3.6	—	500	μA	

AC characteristics (Ta = -40~85°C)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	MIN.	MAX.	UNIT
Maximum Clock Frequency	f _{MAX}	(Fig.1, 2)	2.7	—	—	MHz
			3.3 ± 0.3	150	—	
Propagation Delay Time (CK-Q, \bar{Q})	t _{pLH} t _{pHL}	(Fig.1, 2)	2.7	—	8.0	ns
			3.3 ± 0.3	1.5	7.0	
Propagation Delay Time (CLR, PR-Q, \bar{Q})	t _{pLH} t _{pHL}	(Fig.1, 4)	2.7	—	8.0	ns
			3.3 ± 0.3	1.5	7.0	
Minimum Pulse Width (CK)	t _W (H) t _W (L)	(Fig.1, 2, 3)	2.7	3.3	—	ns
			3.3 ± 0.3	3.3	—	
Minimum Pulse Width (CLR, PR)	t _W (L)	(Fig.1, 2, 3)	2.7	3.6	—	ns
			3.3 ± 0.3	3.3	—	
Minimum Set-up Time	t _s	(Fig.1, 2)	2.7	2.5	—	ns
			3.3 ± 0.3	2.5	—	
Minimum Hold Time	t _h	(Fig.1, 2)	2.7	1.5	—	ns
			3.3 ± 0.3	1.5	—	
Minimum Removal Time	t _{rem}	(Fig.1, 3)	2.7	3.0	—	ns
			3.3 ± 0.3	2.5	—	
Output To Output Skew	t _{osLH} t _{osHL}	(Note 10)	2.7	—	—	ns
			3.3 ± 0.3	—	1.0	

(Note 10) Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

DYNAMIC SWITCHING CHARACTERISTICS (Ta = 25°C, Input t_r = t_f = 2.5ns, C_L = 50pF, R_L = 500Ω)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	UNIT
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V

CAPACITIVE CHARACTERISTICS (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP	UNIT
Input Capacitance	C _{IN}	—	3.3	7	pF
Output Capacitance	C _{OUT}		0	8	pF
Power Dissipation Capacitance	C _{PD}	f _{IN} = 10MHz (Note 11)	3.3	25	pF

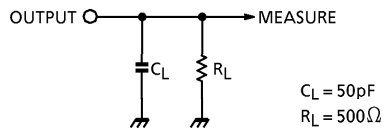
(Note 11) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ (per F/F)}$$

TEST CIRCUIT

Fig.1



AC WAVEFORM

Fig.2 t_{pLH} , t_{pHL} , t_w , t_s , t_h

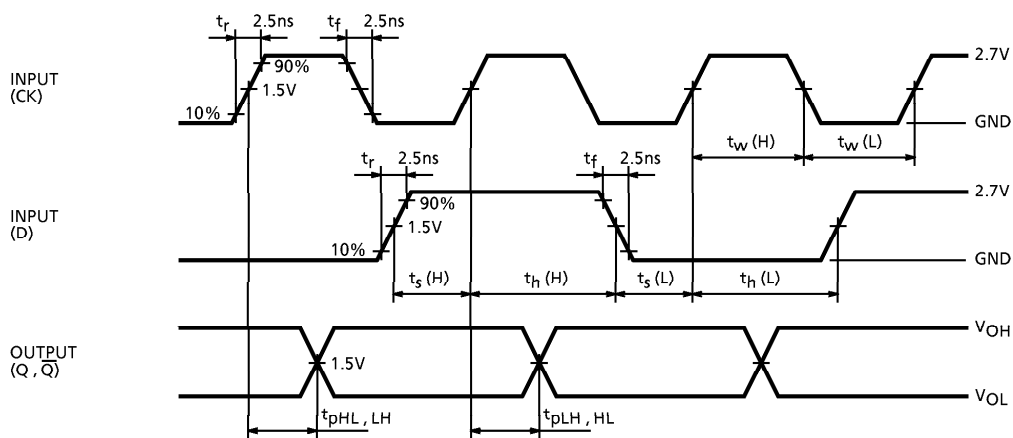


Fig.3 t_{rem}

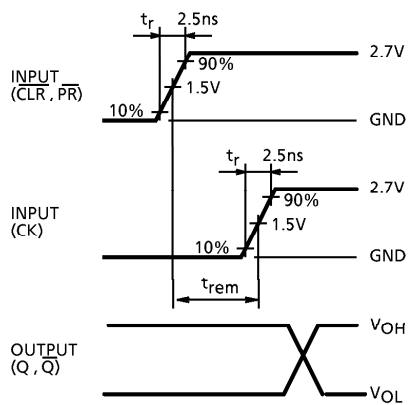
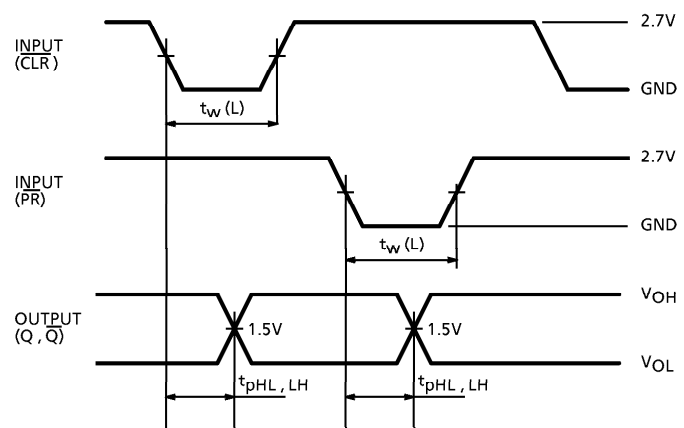
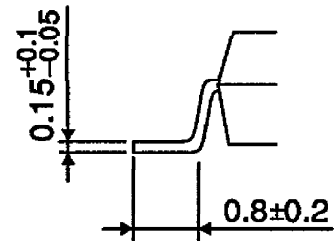
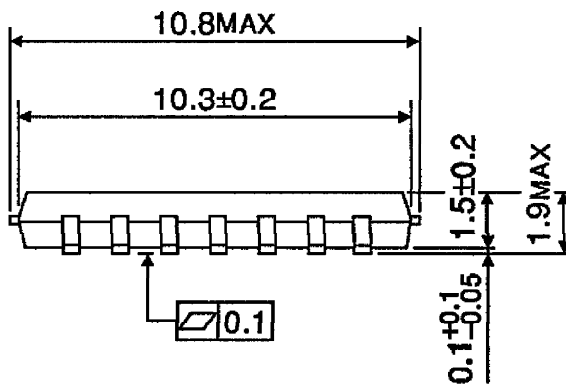
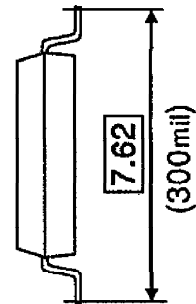
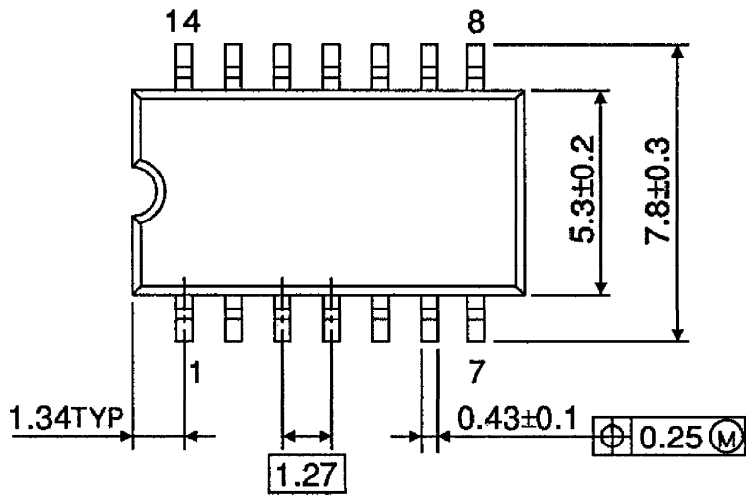


Fig.4 t_{pLH} , t_{pHL}



OUTLINE DRAWING
SOP14-P-300-1.27

Unit : mm

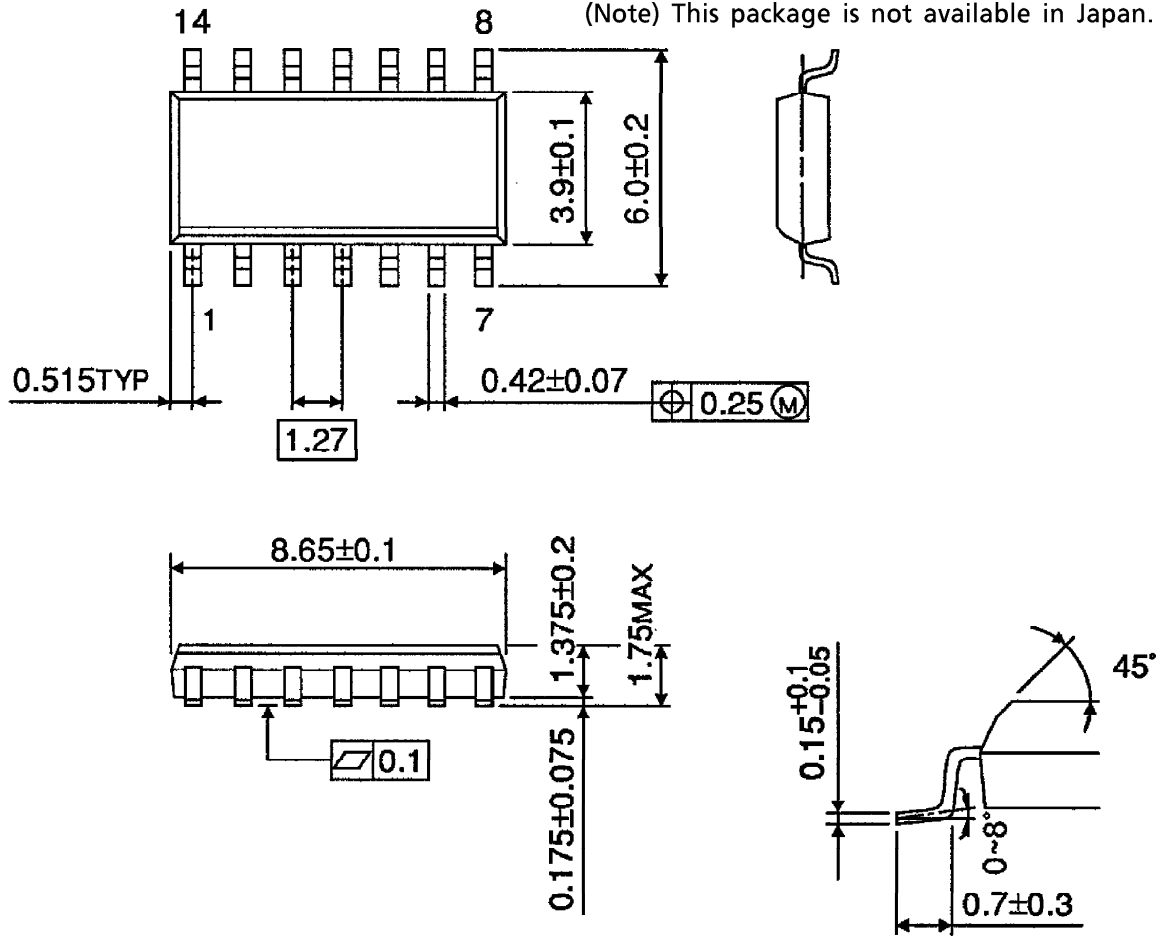


Weight : 0.18g (Typ.)

OUTLINE DRAWING
SOL14-P-150-1.27

Unit : mm

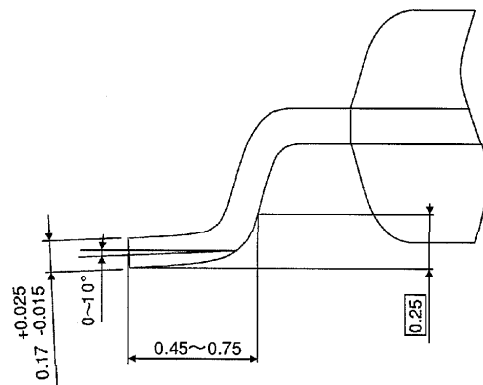
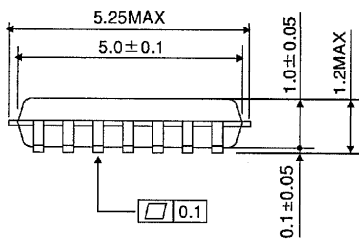
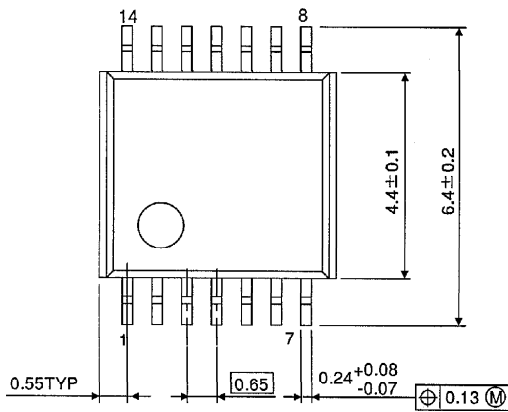
(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

OUTLINE DRAWING
TSSOP14-P-0044-0.65

Unit : mm



Weight : 0.06g (Typ.)